M.Sc(CS) (First Semester) Examination,2013
Digital Electronics
Paper: Fifth

SECTION-A

I) An electronics circuit/ device which manipulates the operation on binary bits such as logical and arithemetic. It has one or more inputs and only one output used for making logical decision is called logic gates. Basic logic gates are AND, OR and NOT

ii) Flip flops in its simplest form is known as latches. Latches are bistable device which can store either o or 1 binary bit. latches can be memory devices, and can store one bit of data for as long as the device is powered.

iii) $(01101110.1000101)_2=(\ 0110\ \ 1110.\ 1000\ \ 1010)_2=(6\ E\ .\ 8\ A)_{16}$

iv) $(\ 0.563)8 = .\ 5\ X\ 8^{-1}+6\ X\ 8^{-2}\ +3\ X\ 8^{-3}$

V) PROM stands for Programmable Read only memory. It can be programmed once. EPROM stands for Erasable programmable memory. Content of this type of ROM can be altered electrically.

vi) $.134522\ X\ 10^{5}$
$+\ .342111\ X\ 10^{3}$

$.\ 137943X\ 10^{5}$

Vii) Drivers are the software which gives information or direct the operating system about how to interact with particular hardware devices. Example: Printer driver, CD driver, graphics adapter, sound card driver etc.

viii) ASCII code stands for American standard code for information inter change. It is a 7 bit code containing 128 characters. ASCII 65 is for the character A. basically ASCII codes are used for representing characters.

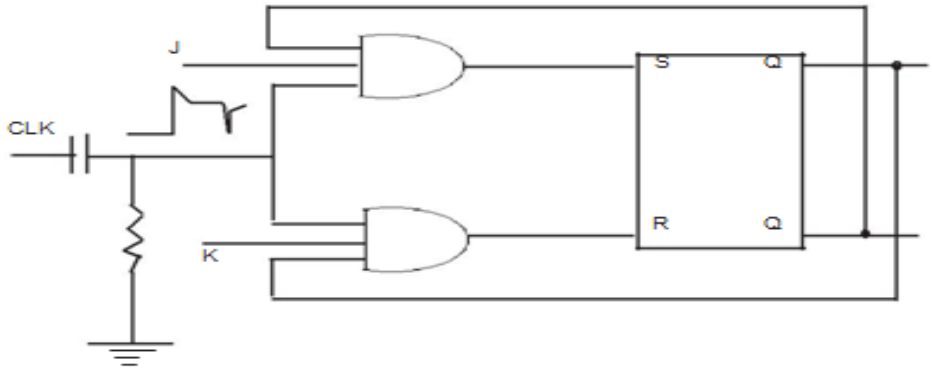
ix) The Short comings of SR flip flop is the undetermined condition (input 11) is never used because its output is undetermined and the input 00 produces no change in the output.

X) $(5B.3A)_{16}$= $(01011011.00111010)_2$= (001 011 011 . 001 110 $100)_2$= (1 3 3. 1 6 $4)_2$

SECTION-B

2. JK FLIP – FLOP

Fig. 2.5 shows one way to build a JK flip – flop the variables J and K are called control inputs because they determine what the flip – flop does on the arrival of a positive clock edge.



CLK	K	L	Q
0	X	X	NC
1	X	X	NC
↓	X	X	NC
X	0	0	NC
↑	0	1	0
↑	1	0	1
↑	1	1	Toggle

Fig2.7 JK flip flop symbol and its truth table.

Inactiver: When J and K are both low, both AND gates are disabled and the circuit is inactive at all times including the rising edge of the clock.

Reset : When J is low and K is high, the upper gate is disabled; so there is no way to set the flip - flop. The only possibility is reset. When Q is high, the lower gate passes a reset trigger as soon as the next positive clock edge arrives. This forces Q to become low. Therefore, J=0 and K=1 means that the next positive clock edge resets the flip-flop.

Set: When J is high and K is low, the lower gate is disabled; So it is impossible to reset the flip-flop. But you can set the flip-flop as follows. When Q is low, Q is high; therefore, the upper gate passes a set trigger on the positive clock edge. This drives Q into the high state. That is , J=1 and K =0 means that the next positive clock edge sets the flip - flop.

Toggle: When J and K both are high (notice that this is the forbidden state with an RS flip - flop), it is possible to set or reset the flip - flop. If Q is high, the lower gate passes a reset trigger on the next positive clock edge. When Q is low, the upper gate passes a set trigger on the next positive clock edge. Either way Q changes to the compliment of the last state. Therefore, J =1 and K=1 means that the flip - flop will toggle on the next positive clock edge.
("toggle" means switch to opposite state)

Clocked RS flip – flop

Two different methods for constructing an RS flip – flop were discussed in the previous section with NOR gate and NAND gate

realization. Both of these RS flip – flops or latches, are said to be "transparent "; that is any change in input at R or S is transmitted immediately to the output at Q and Q thus they acts as short term memory.

It is possible to store or clock the flip – flop in order to store information (set it or reset it) at any time, and then hold the stored information for any desired period of time. This flip – flop is called clocked RS flip – flop.

The circuit of a clocked RS flip – flop is shown in figure 2.6 with its symbol and truth table.

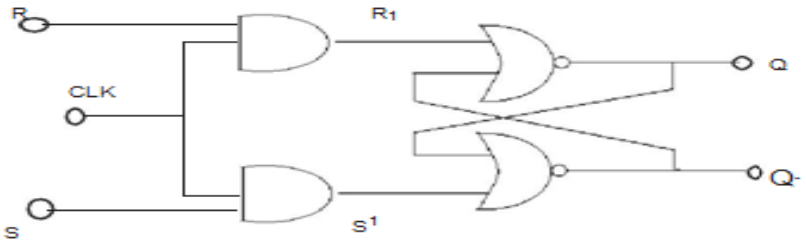


Fig. No. 2.6

CLK	R	S	Q
0	0	0	NC
0	0	1	NC
0	1	0	NC
0	1	1	NC
1	0	0	NC
1	0	1	1
1	1	0	0
1	1	1	* (Race)

Clocked RS flip – flop x symbol and its truth table

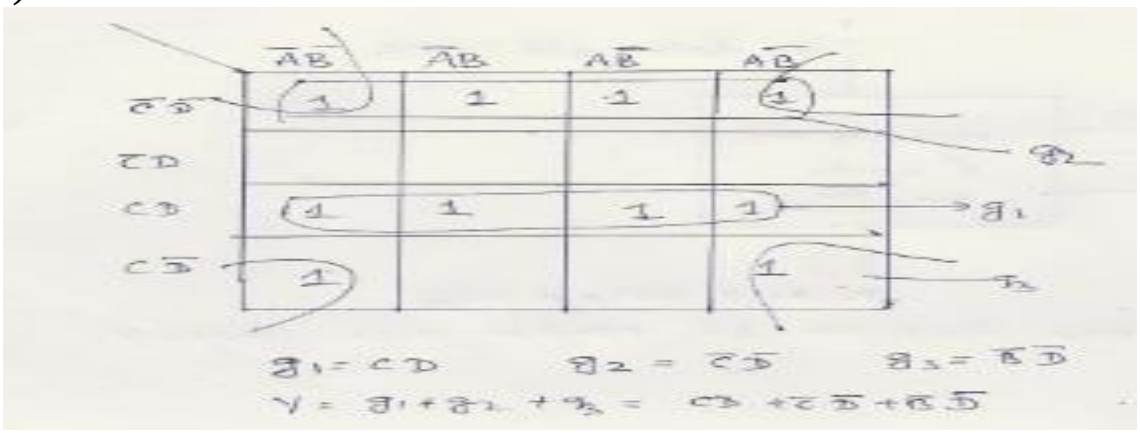
It consists of two additional and gates added at the input of R S flip – flop. In addition to control inputs R and S, there is a clock input CK.

The output of the two and circuits (S^1 and R^1) will be 0 as long as CK = 0. then the state of the flip – flop will remain unchanged and if S = 0 , R = 1

then S = 0 R = 1 and the flip – flop is reset to 0. On the other hand if S = 1 , R = 0 then S =1 R = 1 and the flip flop is set to 1. the presence of R^1 =1 and S^1 =1 , will however , results in an undetermined state.

3.

i)



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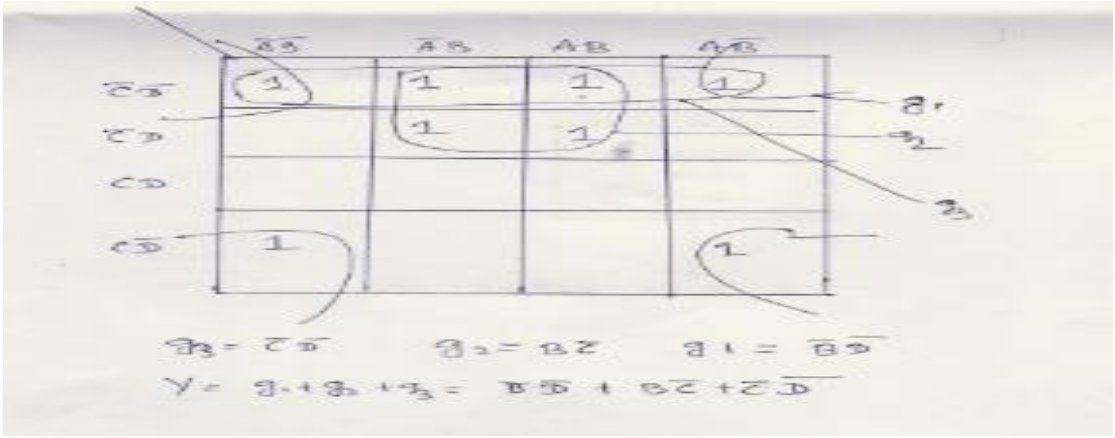
ii)

Y= ABD(C+C')+AC'D'(B+B')+A'BC'(D+D')+ABC'D+AB'CD'

=ABCD + ABC'D + ABC'D'+AB'C'D'+A'BCD+A'BC'D'

+ ABC'D + AB'CD'



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4. (Any three differences of each)

Static RAM : 1. Used for cache memory.

2.Very cost effective.

3. Access time is faster

4. less storage space

Dynamic Ram 1. Used for main memory

2. Cost is less than SRAM

3. Access time is less as compared to SRAM

4. Storage capability is high.

Primary memory: 1. Access speed is high.

2. Less storage capacity.

3. Primary memories are internal memory.

4. May be volatile or non volatile.

Secondary memory:1. Access speed is slow

2. High storage capacity

3. Secondary memories are external.

4. Secondary memories are non volatile memories.

Main memory: 1. Storage capacity is high

2. High access speed

3.Constructed from DRAMs

4. Stores currently used data.

Cache memory: 1. Storage capacity is low

2. low access speed

3. Constructed from SRAM

4. Stores frequently used data.

Multiplexer: 1. It is a digital circuit which takes n input data line and selects one out of them or produces one output line.

2.Many input and one output.

De multiplexer: 1.It is a digital circuit which takes one data input line and places the data on any of 2^n output lines.

2.One input line and many output line.

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5. **SEMICONDUCTOR MEMORIES**

Recent developments in semiconductor technology have provided a number or reliable and economical MSI and LSI memory circuits. The typical semiconductor memory consists of a rectangular array of memory cells. The basic memory cell is typically a transistor flip flop or a circuit capable of storing charge and used to store 1 bit of

information. The two general categories of semiconductor memories are RAM and ROM. They can be further divided into various types as illustrated as follows

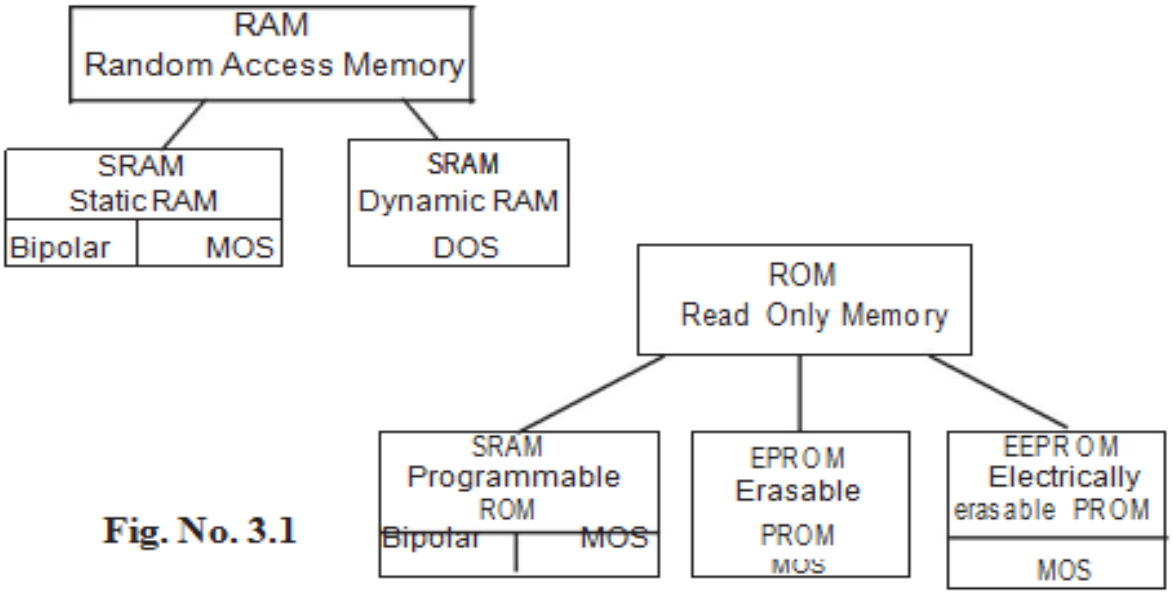


Fig. No. 3.1

Memory Terminology:

Read only memories come in four versions. The standard ROM is programmed by the manufacturer. The PROM can be programmed permanently by the user or manufacturer using special equipment. It can be programmed only once. The EPROM (Erasable Programmable Read Only Memory) can be programmed and erased by the user. Stored data in EPROM can be erased by passing high – intensity ultraviolet light through a special transparent window in the top of the IC. Another erasable PROM is the EEPROM (electrically Erasable Programmable Read Only Memory) . The EEPROM can be erased and programmed by the user with special equipment. It is erased electrically rather than with ultraviolet light. All the types of ROM s

are non volatile light. All the types of ROM s area non volatile, which means they will not lose their data when power to the IC is turned off:

PROMS AND EPROMS: The term ROM is generally reserved for memory chips that are programmed by the manufacturer. You have to send a list of data to be stored in the different memory locations to the manufacturer, who then produce a mask. Now the user can be able to read the stored. Data from the ROM.

Programmable: A programmable ROM(PROM) is different. It allows the user to store the data. An instrument called a PROM programmer is used in storing the data(also called "burning in"). once this has been done, the programming is permanent, that is the stored bits cannot be erased.

Erasable: The erasable PROM(EPROM) used MOSFETs. Data is stored with a PROM programmer. Later , data can be erased with ultraviolet light passing through a window present on the top of memory chip. This releases stored charges and the effect is to wipe out the stored contents. The user can erase and store until the program and data are perfected.

EEPROM: Another type of reprogrammable ROM device is the EEPROM (Electrically Erasable Read Only Memory). It is a non volatile like EPROM but does not require ultraviolet light to erase the data. It can be erased by using electrical pulses. It can be used for slower

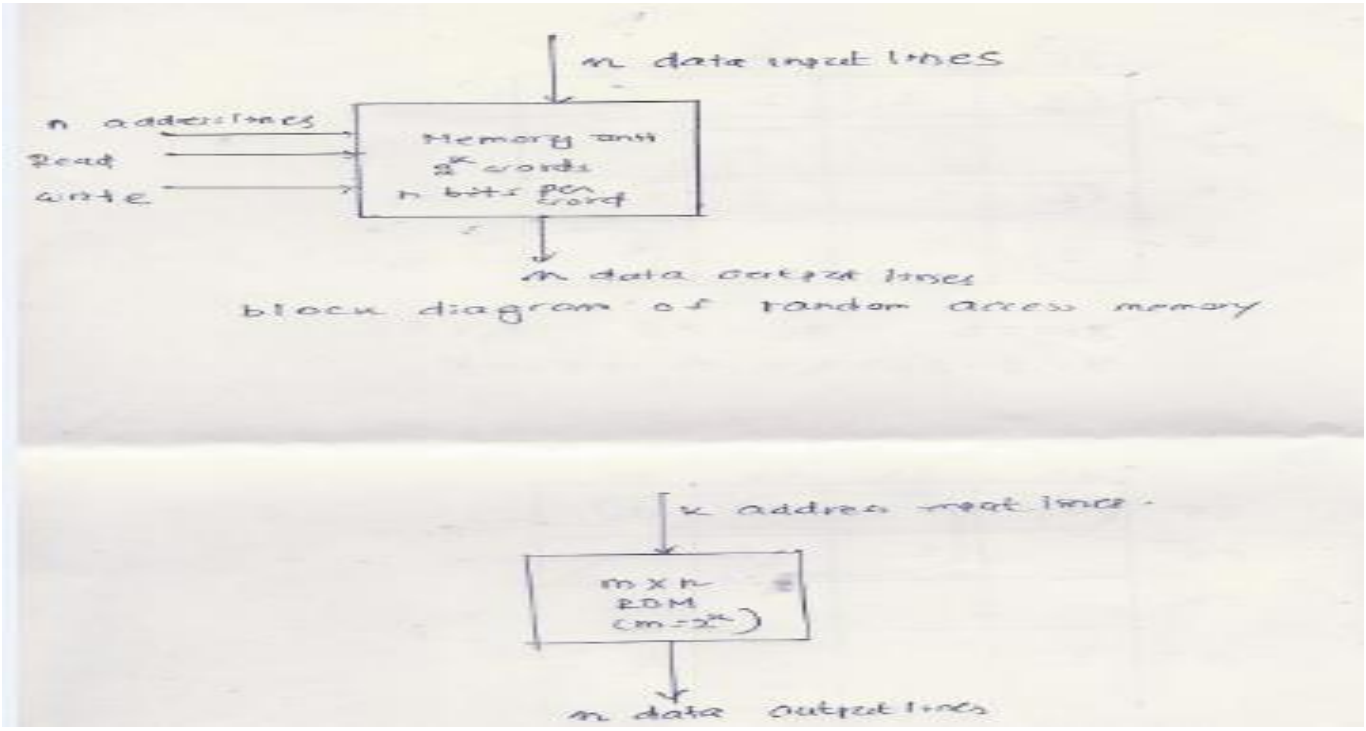
Semi conductor RAM's: Semiconductor RAMs may be static or

dynamic.

Static RAM: Static RAM retain stored information only as long as the power supply is on**.** The static RAM uses bipolar or MOS flip – flops . Static memory are cost effective. It consumes much power . they do not need re refreshing circuitry

Dynamic RAM: A dynamic RAM may contain thousand of memory cells like this. The stored data must be refreshed (Recharged) for every few milliseconds. Because the capacitor charge leaks off. Since memory cells than a static RAM of the same physical size. The disadvantage of dynamic RAM is the need to refresh the capacitor charge every few milliseconds. Dynamic RAMS are cheaper

Figures for RAM and ROM



Secondary memory with diagrams:

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6. a Various types of codes (Any three)

EBCDIC code : It is extended binary coded decimal interchange code. It is the standard character code for larger computer. It is an 8 bit code without parity. A ninth bit can be used for parity. With 8 its up to 256 characters can be coded.

Gray codes: In gray codes there is only one bit changes at a time when a transition is made from one number to another:

gray codes : 0000, 0001,0011, 0010,…….

Excess three codes: Excess three codes are unweighted codes . Ther are formed by adding three to a binary number. Excess three code of 4 is 4+3 = 7
Example : 101 (5)→1000 in excess three code.

The ASCII code: To get information into and out of a computer, we need to use numbers, letters, and other symbols. This implies some kind of alphanumeric code for the I/O unit of a computer. At one time, every manufacturer had a different code, which led to all kinds of confusion. Eventually, industry settles on a input – output code known as the American Standard code for Information Interchange (abbreviated ASCII). This code allows manufacturers, to standardize I/O hardware such as keyboards, Printers, video displays, and so on. It is a 7 bit code consisting of 128 characters.

Ascii code also contains 8 bit including the parity bit.
Other codes are BCD codes , Excess three codes.

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6. b. 1. X+Y=Y+X
2. X.Y=Y.X
3. X(YZ)=(XY)Z=XYZ
4. X+XY=X
5. X(X+Y) =X
6. X(Y+Z)=XY+XZ
7. XY+XY'=X
8. (X+Y)+Z=X+(Y+Z)=X+Y+Z
9. X+Y.Z = (X+Y)(X+Z)
10. (X+Y)(X+Y')=X

7.b 4-Bit binary counter:

A register that goes through a predetermined sequence of steps up on the application of input pulses is known as counters.A counter that follows binary sequence is called binary counter. A n bit counter is a register of n Flip flops and associated gates. A binary counter goes through the sequence of binary number 0000,0001,….1111. Every lower order bit is complemented after the next sequence . Ex- Binary count 0111 to 1000 is obtained by a) complementing the lower order bit b) complementing the second order bit because the first two bits of 0111 is 1 and complementing 4^{th} bit because all previous bits are 1

A 4 bit binary counter can be implemented by By using JK FF. JK FF has the property of toggling when the inpts are 11 and No change when

the inputs are 00. In addition the counter is controlled by using an enable input that turns the counter on or off. If the JK input is maintained at 00 there is no change in output. Wnen the enable input is 1 The lower order bit changes to 1 and rest of the bits doesnot change giving rise to the sequence 0001. The next clock pulses results 0010……..1111.

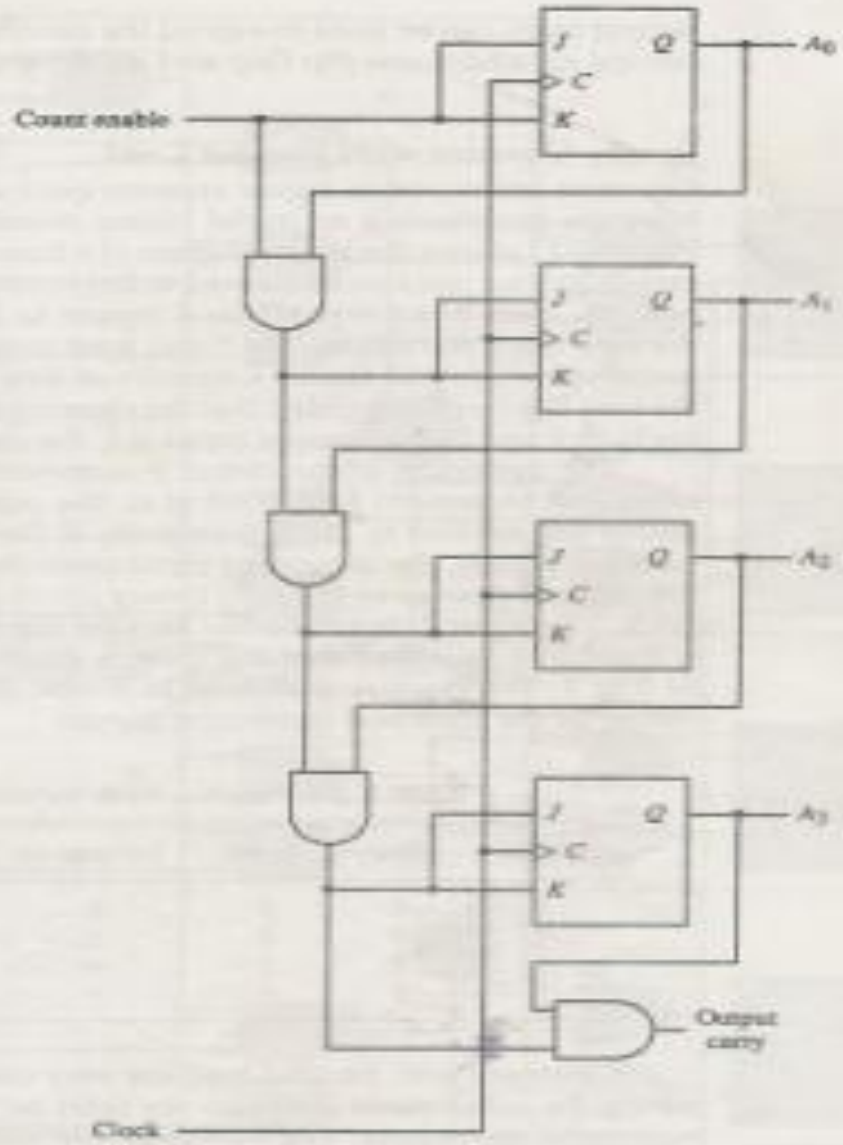

Figure 2-10 4-bit synchronous binary counter.

at 0 and the output of the counter does not change. The first stage A_0 is complemented when the counter is enabled and the clock goes through a positive transition. Each of the other three flip-flops are complemented when all previous least significant flip-flops are equal to 1 and the count is enabled. The chain of AND gates generate the required logic for the *J* and *K* inputs. The

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7.b

Registers: A register is a group of flip-flops capable of storing one bit of information. An n bit register has agroup of n flip-flop and capable of storing any binary information of n bits. 4 bit register consists of 4 D flip flops with common clock pulses . The clear input goes to special input of flip flops. When input goes to 0 all FFs reset. Clear input is used for clearing the register.

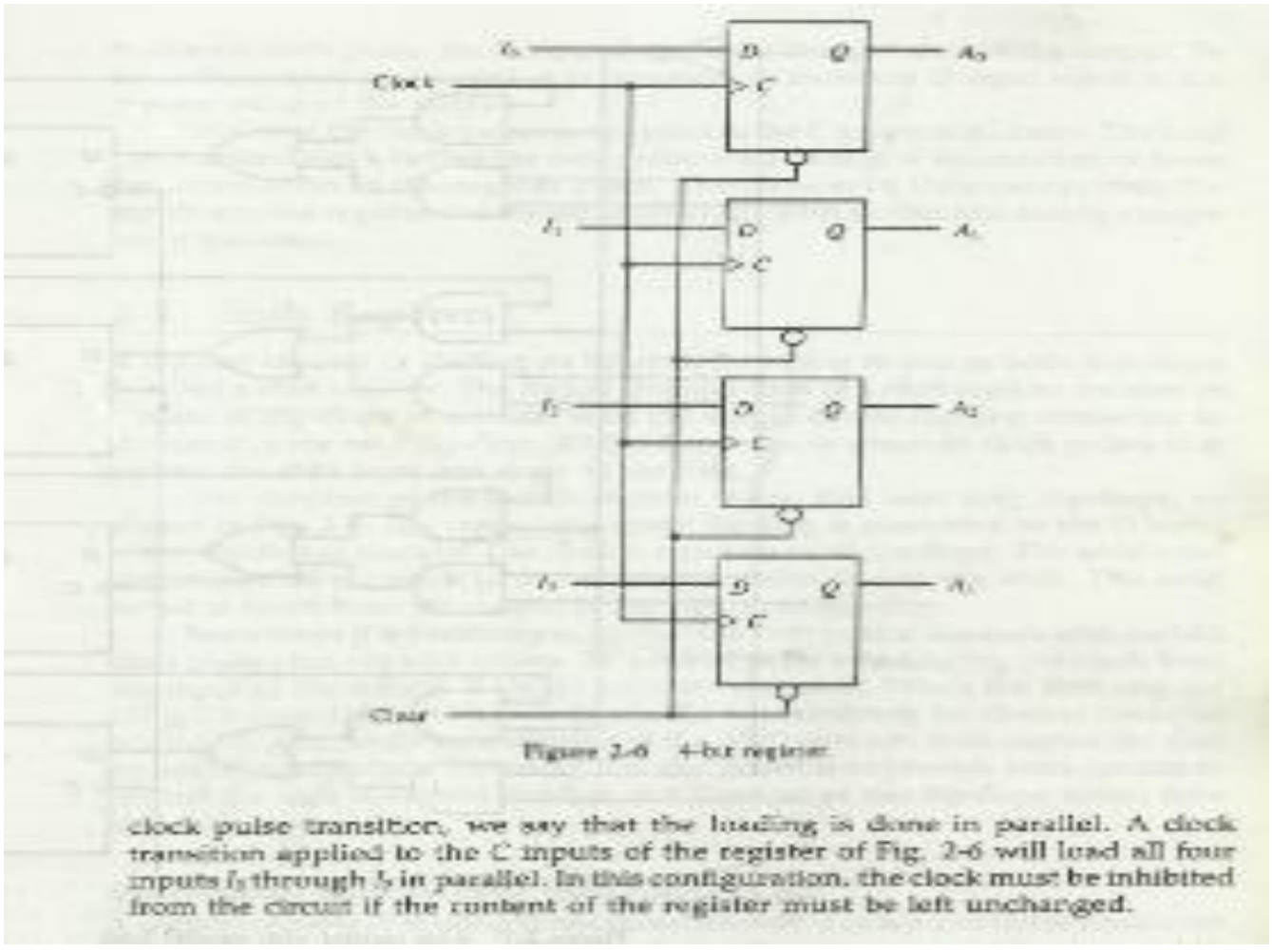

Figure 2-6 4-bit register

clock pulse transition, we say that the loading is done in parallel. A clock transition applied to the C inputs of the register of Fig. 2-6 will load all four inputs I_3 through I_0 in parallel. In this configuration, the clock must be inhibited from the circuit if the content of the register must be left uncharged.

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8 a. Digital Integrated Circuits:

The digital IC technology has advanced considerably and rapidly over the years.Starting from small scale integration (SSI) with less than 12 gates per chip ,advancing to medium scale integration (MSI)with 12 to 100 gates per chip and then to large scale integration (LSI) with up to 10,000 gates per chip and on to Very large scale integration (VLSI) with up to 100,000 gates per chip,the digital IC technology has come a long way.Recently it has advanced to ultra large scale integration(ULSI) with more than 100,000 gates per chip. A group of compatible ICs with similar logic levels and supply voltages fabricated using a specific circuitary is referred as a logic family.

Based on the technology used ,we can have seven basic logic families.They are:

1.RTL- Resistor transistor logic family

2.DTL- Diode transistor logic family

3.IIL- Integrated injection logic family

4.TTL- Transistor transistor logic family

5.ECL- Emitter coupled logic family

6.MOS -Metal oxide semiconductor logic family

7.CMOS- Complementary metal oxide semiconductor logic family.

Among these families we consider here RTL,DTL,ECL,TTL and CMOS logic families only.

1.4.1 Characteristics: The basic characteristics of a logic family are :

(i). Speed of operation,

(ii) Fan-in and Fan-out,

(iii) Power dissipation,

(iv) Propagation Delay,

(v) Operating temperature range,

(vi) Voltage and Current parameters and

(vii) Noise margin(Noise immunity)

8.b. Logic gates: Circuits used to process digital signals are called logic gates. Logic symbols are used to identify these circuits. They have one or more input signals but only one output signal. Gates are often called logic circuits because they can be analyzed with Boolean algebra

As well as a standard Boolean Expression, the input and output information of any **Logic Gate** or circuit can be plotted into a table to give a visual representation of the switching function of the system and this is commonly called a **Truth Table**. A logic gate truth table shows each possible input combination to the gate or circuit with the resultant output depending upon the combination of these input(s).

For example, consider a single **2-input** logic circuit with input variables labeled as A and B. There are "four" possible input combinations or 2^2 of "OFF" and "ON" for the two inputs. However, when dealing with Boolean expressions and especially logic gate truth tables, we do not general use "ON" or "OFF" but instead give them bit values which represent a logic level "1" or a logic level "0" respectively.

Then the four possible combinations of A and B for a 2-input logic gate is given as:

- Input Combination 1. - "OFF" - "OFF" or (0, 0)
- Input Combination 2. - "OFF" - "ON" or (0, 1)
- Input Combination 3. - "ON" - "OFF" or (1, 0)
- Input Combination 4. - "ON" - "ON" or (1, 1)

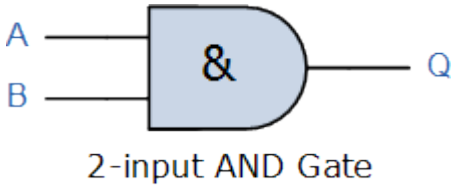
Therefore, a 3-input logic circuit would have 8 possible input combinations or 2^3 and a 4-input logic circuit would have 16 or 2^4, and so on as the number of inputs increases. Then a logic circuit with "n" number of inputs would have 2^n possible input combinations of both "OFF" and "ON". In order

to keep things simple to understand, we will only deal with simple **2-input** logic gates, but the principals are still the same for gates with more inputs.

The Truth tables for a 2-input AND Gate, a 2-input OR Gate and a NOT Gate are given as:

2-input AND Gate

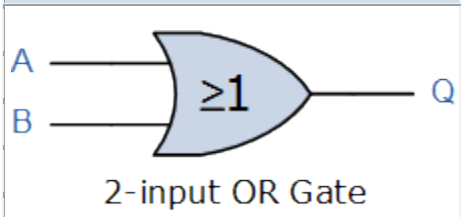
For a 2-input AND gate, the output Q is true if BOTH input A "AND" input B are both true, giving the Boolean Expression of: (Q = A and B).

Symbol	Truth Table		
	A	B	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A.B	Read as A **AND** B gives Q		

Note that the Boolean Expression for a two input AND gate can be written as: A.B or just simply AB without the decimal point.

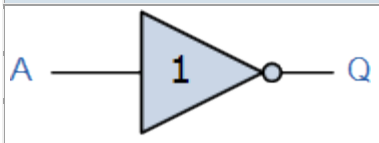
2-input OR (Inclusive OR) Gate

For a 2-input OR gate, the output Q is true if EITHER input A "OR" input B is true, giving the Boolean Expression of: (Q = A or B).

Symbol	Truth Table		
	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression Q = A+B	Read as A **OR** B gives Q		

NOT Gate

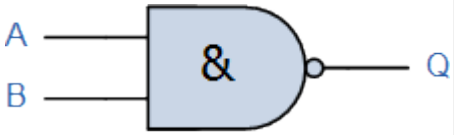
For a single input NOT gate, the output Q is ONLY true when the input is "NOT" true, the output is the inverse or complement of the input giving the Boolean Expression of: (Q = NOT A).

Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0
Boolean Expression Q = NOT A or A	Read as inverse of A gives Q	

The NAND and the NOR Gates are a combination of the AND and OR Gates with that of a NOT Gate or inverter.

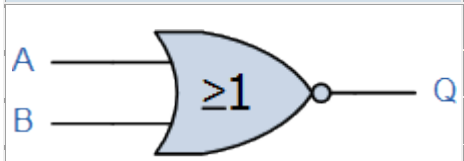
2-input NAND (Not AND) Gate

For a 2-input NAND gate, the output Q is true if BOTH input A and input B are NOT true, giving the Boolean Expression of: (Q = not(A and B)).

Symbol	Truth Table		
 2-input NAND Gate	A	B	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A .B	Read as A **AND** B gives NOT-Q		

2-input NOR (Not OR) Gate

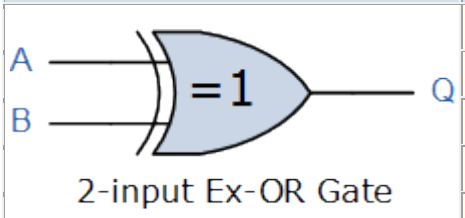
For a 2-input NOR gate, the output Q is true if BOTH input A and input B are NOT true, giving the Boolean Expression of: (Q = not(A or B)).

Symbol	Truth Table		
 2-input NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	0
Boolean Expression Q = A+B	Read as A **OR** B gives NOT-Q		

As well as the standard logic gates there are also two special types of logic gate function called an Exclusive-OR Gate and an Exclusive-NOR Gate. The actions of both of these types of gates can be made using the above standard gates however, as they are widely used functions, they are now available in standard IC form and have been included here as reference.

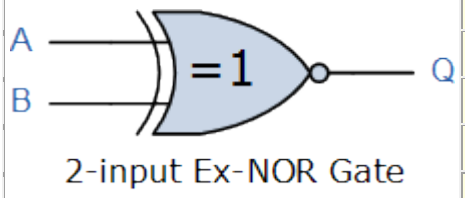
2-input EX-OR (Exclusive OR) Gate

For a 2-input Ex-OR gate, the output Q is true if EITHER input A or if input B is true, but NOT both giving the Boolean Expression of: (Q = (A and NOT B) or (NOT A and B)).

Symbol	Truth Table		
 2-input Ex-OR Gate	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A⊕B			

2-input EX-NOR (Exclusive NOR) Gate

For a 2-input Ex-NOR gate, the output Q is true if BOTH input A and input B are the same, either true or false, giving the Boolean Expression of: (Q = (A and B) or (NOT A and NOT B)).

Symbol	Truth Table		
 2-input Ex-NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A ⊕ B			

Summary of all the 2-input Gates described above.

The following Truth Table compares the logical functions of the 2-input logic gates above.

Inputs		Truth Table Outputs for each Gate					
A	B	AND	NAND	OR	NOR	EX-OR	EX-NOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

The following table gives a list of the common logic functions and their equivalent Boolean notation.

Logic Function	Boolean Notation
AND	A.B
OR	A+B
NOT	A
NAND	A .B
NOR	A+B
EX-OR	(A.B) + (A.B) or A⊕B
EX-NOR	(A.B) + or A ⊕ B

2-input logic gate truth tables are given here as examples of the operation of each logic function, but there are many more logic gates with 3, 4 even 8 individual inputs. The multiple input gates are no different to the simple 2-input gates above, So a 4-input AND gate would still require ALL 4-inputs to be present to produce the required output at Q and its larger truth table would reflect that.
